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EXAMINER	
SMITH, CHENEA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/699,311	FYE, JAMES C.	
	Examiner	Art Unit	
	CHENEA P. SMITH	2421	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to communications filed 12/28/2009. Claims 1-2, 7, 14 and 19 are amended. Claim 29 is cancelled. Claims 1-28 are pending in this action.

Response to Arguments

2. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

3. Although a new ground of rejection has been made, a response is considered necessary for several of Applicant's arguments, specifically since the Reitmeier, Miura, Reynolds and Kovacevic references will continue to be used.

4. In response to Applicant's arguments on page 12, lines 16-23 that "*Applicant respectfully points out that an Intraframe is a complete frame of video data as opposed to a B-frame or a P-frame which contains only changed data from the last I-frame. As such, Reitmeier is not describing the "decoding of a scaled field of a frame in the video data" because an I-frame is a complete video data frame and not just a field from a frame. Moreover, in reviewing Reitmeier Applicant is unable to discern any sections in Reitmeier teaching or suggesting such elements. Therefore, Reitmeier fails to cure the defects of Machida and Reynolds'. Therefore, claim 13 is allowable over the combination of Machida, Reynolds" and Reitmeier for at least this additional*

and independent reason", the Examiner respectfully disagrees. As a field makes up, i.e., is a portion of, a frame, since the frame of Reitmeier is scaled, the field of the frame is therefore scaled. Therefore, this reasonably meets the limitation of decoding a scaled field of a frame in the video data, as claimed.

5. In response to Applicant's arguments on page 14, lines 4-11 that "*Further, in regard to claim 25, the Examiner rejects claim 25 by asserting that the combination of Machida and Reynolds" describes most of the claim elements but concedes that the combination Machida and Reynolds" fails to describe that "the video fail operation comprises an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure." The Examiner proceeds in his rejection by asserting that Miura cures the conceded discrepancy and cites Column 20; lines 49-54 and Column 36; lines 20-33 in support. However, Applicant respectfully points out that Miura fails to describe the subject matter subscribed to Miura",* the Examiner respectfully disagrees. In addition to col 20, lines 49-54 and col 36, lines 20-33, for clarification, the Applicant should please note that Miura discloses that in the event of a failure, a previous image (see col 21, lines 51-60 and Fig. 2C) is displayed, and that this process may be combined (see col 39, lines 15-16) with the step of including a type of special data in the event of a failure, such as a message of no input, etc. (see col 20, lines 46-53).

6. In response to Applicant's arguments on page 15, lines 6-13 that "*For example, the Examiner has stipulated that the Reynolds processes that allegedly reading on the Applicant's base claims all take place in the interactive set top boxes 112/118, which process strictly digital data. As can be seen form Figure 1 of Reynolds, all analog data is converted to digital data prior to being transmitted by Digital Video Distribution Network 104. Therefore, no processes*

occurring in the User's Locations 111 are capable of processing analog data. As such, a prima facie case of obviousness cannot be established because there is no motivation to modify Reynolds" (digital processing) by Kovacevic (using analog data) because there is no reasonable chance of success in processing analog data by digital circuitry (See, MPEP §2143.02)", the Applicant should please note that a reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments (see MPEP 2123). While Reynolds may disclose a digital distribution network, he also discloses that his "distribution network 104 may comprise a cable television network, satellite television network, internet video distribution network, or any other network capable of distributing video data" (see [0027], lines 4-8), which then must include any modifications and variations in light of his teachings (see Reynolds, [0061], lines 1-6), and thereby provides a reasonable motivation to modify his system in view of Kovacevic.

7. In response to Applicant's arguments on page 15, lines 16-21 that "*similarly, the Examiner has stipulated that the Machida processes that allegedly read on the Applicant's base claims all occur in the image selection means 100, which processes strictly digital data. As can be seen form FIG. 4 of Machida, all video analog data is converted to digital data at A/D converter 213, prior to being transmitted to the digital image selection means 100. Therefore, no processes occurring in the image selection means are capable of processing analog data. As such, a prima facie case of obviousness cannot be established because there is no motivation to modify Machida (digital processing) by Kovacevic (using analog data) because there is no reasonable chance of success in processing analog data by digital circuitry (See, MPEP*

§2143.02)", the Applicant should please note that Fig. 3, which does not show a processing of strictly digital data, and not Figure 4 of Machida was used to meet the limitations of the claims.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4-5, 7-8, 11-12, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome et al. (US20020078447, hereinafter Mizutome).

Regarding claims 1, 7 and 19, Machida discloses an apparatus for display of video data (image generation apparatus 100, see Fig. 3), the apparatus comprising:

a switch network (image selection means 101, see Fig. 3) including an output (see Fig. 3) and an input (see Fig. 3), and

a plurality of video processing pipelines (image processing means 102, see Fig. 3), each video processing pipeline including an input coupled to the switch network output (see Fig. 3), wherein the switch network is configured to connect any of the switch inputs to any of the video processing pipeline inputs (see Fig. 3).

Machida does not specifically disclose a plurality of video sources,

a plurality of video channels configured to be coupled to different video sources,

a plurality of video decoders coupled to the plurality of video channels, each video decoder coupled to a different one of the plurality of video channels and comprising:

an output,

an input coupled to one or more video channels, to receive video data from the one or more video channels, and to decode the received video data, or

a manual I/O interface in operable communication with the plurality of video processing pipelines, the manual I/O interface configured to provide an option to a user to direct the switch network to connect a specific video decoder output to a particular view window of the apparatus for display.

In an analogous art, Reynolds discloses a plurality of video sources (see Fig. 1),

a plurality of video channels configured to be coupled to different video sources (see Fig. 1),

a plurality of video decoders (video decoders 220/224/228, see Fig. 2) coupled to the plurality of video channels (see Fig. 2), each video decoder coupled to a different one of the plurality of video channels (see Fig. 2) and comprising:

an output (see Fig. 2), and

an input coupled to one or more video channels (see Fig. 2), to receive video data from the one or more video channels (see Figs. 1-2), and to decode the received video data (see Fig. 2).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Machida's system to include the limitations as taught by Reynolds for the

advantage of providing an improved system capable of combining multiple video signals at a user location to effectively display multiple images.

Machida in view of Reynolds does not specifically disclose a manual I/O interface in operable communication with the plurality of video processing pipelines, the manual I/O interface configured to provide an option to a user to direct the switch network to connect a specific video decoder output to a particular view window of the apparatus for display.

In an analogous art, a manual I/O interface (user interface 124/remote controller 125, see Mizutome, Figs. 1 and 2) in operable communication with a plurality of video processing pipelines (see Mizutome, Fig. 1), the manual I/O interface (user interface 124/remote controller 125, see Mizutome, Figs. 1 and 2) configured to provide an option to a user to direct a network to connect a specific video decoder output to a particular view window of an apparatus for display (Mizutome discloses that a user may use the remote control to choose from various screen layout selections in which various input sources may be viewed in different windows, positions, etc. {see Mizutome, [0082], lines 1-8, [0104], lines 1-6 and Fig. 4}, and also that a user may alter a screen layout into a suitable format for viewing and listening, i.e., alter the screen layout so that a particular source is view in a specific window{see Mizutome, [0105], lines 1-5 and Fig. 4 and Fig. 20}).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds to include the limitations as taught by Mizutome for the advantage of providing an improved system capable of combining multiple video signals at a user location to effectively display multiple images in an output mode preferred by a user (see Mizutome, [0013]).

Regarding claim 4, Machida in view of Reynolds and Mizutome discloses a plurality of video processing pipelines (image processing means 102, see Machida, Fig. 3) configured to process decoded video data (the decoded video data of Reynolds, see Fig. 2, corresponds to the image inputs of Machida) of a plurality of video sources (see Reynolds, Fig. 1) received from a plurality of video decoders (see Reynolds, Fig. 2).

Regarding claims 5, 8 and 22, Machida in view of Reynolds and Mizutome discloses a greater number of video decoders than video processing pipelines (Machida discloses that the images selected to be output may be less than the images input, and therefore the plurality of video processing means are respective to the images selected to be output, see Machida, col 5, lines 28-41 and Fig. 3; since the image inputs of Machida correspond to the video decoder outputs of Reynolds, Machida in view of Reynolds reasonably teaches a greater number of video decoders than video processing pipelines) and wherein the apparatus further comprises a display/control logic (screen control means 106, see Machida, Fig. 3) configured to control a process order of the video data from the plurality of video sources (see Machida, col 5, lines 17-19).

Regarding claim 11, Machida in view of Reynolds and Mizutome discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, a frame in the video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2).

Regarding claim 12, Machida in view of Reynolds and Mizutome discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, a field of a frame in the video data (since an entire video signal is decoded, a

frame of video is therefore decoded, and therefore a field of a frame is decoded, see Reynolds, Fig. 2).

10. Claims 2-3 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claims 1 and 19 above, and further in view of Itoh (of record).

Regarding claims 2 and 20, Machida in view of Reynolds and Mizutome discloses an image size/location logic (image selection means 101/adapted image synthesization means 105/screen control means 106, see Machida, Fig. 3) coupled between the manual I/O interface (as the manual I/O interface of Mizutome is connected to the system via a CPU bus, which would reasonably correspond to the screen control means 106 of Machida, it is reasonably taught that the image size/location logic is coupled between the manual I/O interface, see Mizutome Fig. 1 and Machida, Fig. 3) and each video processing pipeline output (see Machida, Fig. 3), the image size/location logic configured to receive a signal indicating designated size of a display window (display window size must be designated since the sizes of the images are designated in proportion to the screen size, see Machida, col 5, lines 17-27), the image size/location logic further configured to determine a location in the display window (see Machida, col 5, lines 56-58 and col 6, line 1) and a size of a part of the display window for display for the video data (see Machida, col 5, lines 17-23) for each of the plurality of video sources (see Reynolds, Fig. 2) including video data for display (see Machida, col 5, lines 17-23).

Machida in view of Reynolds and Mizutome does not specifically disclose an indication of which of a plurality of video sources includes video data for display in a display window.

In an analogous art, Itoh discloses an indication of which of a plurality of video sources includes video data for display in a display window (see col 12, lines 53-60).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Itoh, for the advantage of conserving the processing resources of the system by only providing only the necessary processing for specific signals.

Regarding claims 3 and 21, Machida in view of Reynolds and Mizutome, and further in view of Itoh discloses a plurality of scalers (image processing means 102, see Machida, Fig. 3) coupled to a plurality of video decoders (see Dawson, Fig. 1A) and a plurality of video processing pipelines (see Machida, Fig. 3), wherein the plurality of scalers are each configured to scale decoded video data from the plurality of video sources (see Machida, col 5, lines 36-41 and Fig. 3) based on the determined size of the part of the display window (see Machida, col 5, lines 17-23).

11. Claims 6, 9-10 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claims 1 and 7 above, and further in view of Miyazaki (of record).

Regarding claims 6 and 27, Machida in view of Reynolds and Mizutome discloses a plurality of video processing pipelines, a plurality of video sources and processed decoded data,

but does not specifically discloses a memory device, or a write multiplexer coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device.

In an analogous art, Miyazaki discloses a memory device (VRAM 18A, see Fig. 1), and a write multiplexer (mux 12, see Fig. 1) coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device (see Fig. 1).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Miyazaki for the advantage of sequentially storing I-frames as they are decoded, thereby reducing the latency of switching signals.

Regarding claim 9, Machida in view of Reynolds and Mizutome, and further in view of Miyazaki discloses storing a processed decoded portion of video data into a portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 10, Machida in view of Reynolds and Mizutome, and further in view of Miyazaki discloses switching the portion of the video buffer that is not updating the display with a portion of the video buffer that is updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14), upon determining (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14) that the plurality of video processing pipelines (see Machida, Fig. 3) has completed processing the decoded portion of the video data (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 28, Machida in view of Reynolds and Mizutome, and further in view of Miyazaki discloses a clock multiplier network (see Miyazaki, col 13, line 35), the clock

multiplier network controlling a rate of operation of the write multiplexer (see Miyazaki, col 13, lines 35-37).

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claim 7 above, and further in view of Reitmeier (of record).

Regarding claim 13, Machida in view of Reynolds and Mizutome discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, but does not specifically disclose decoding a scaled field of a frame in the video data.

In an analogous art, Reitmeier discloses decoding a scaled field of a frame in the video data (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Reitmeier for the advantage of conserving memory resources.

13. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record), Reitmeier (of record), Miyazaki (of record) and Mizutome (previously cited).

Regarding claim 14, Machida discloses a method for displaying video data, comprising:

inputting an image into a first video processing pipeline (image processing means 102, see Fig. 3) via a non-blocking switch network (image selection means 101, see Fig. 3);

inputting a second image into a second video processing pipeline (image processing means 102, see Fig. 3) via the non-blocking switch network (image selection means 101, see Fig. 3);

processing, by the first video processing pipeline the first image (see Fig. 3);

processing, by the second video processing pipeline the second image (see Fig. 3).

Machida does not specifically disclose receiving a first video data from a first video source at a first video decoder via a first video channel;

receiving a second video data from a second video source at a second video decoder via a second video channel;

decoding, via the first video decoder, a first frame of the first video data;

decoding, via the second video decoder, a second frame of the second video data;

inputting the first decoded frame into an image into a first video processing pipeline via a non-blocking switch network;

inputting the second decoded frame into a second image into a second video processing pipeline via the non-blocking switch network;

processing, by the first video processing pipeline the first image decoded frame;

processing, by the second video processing pipeline the second image decoded frame;

transmitting the processed first decoded frame into a first portion of a video buffer for updating the display with the processed first decoded frame;

storing the second processed decoded frame into a second portion of the video buffer that is not updating the display, or

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Reynolds discloses receiving a first video data from a first video source at a first video decoder via a first video channel (see Fig. 1);

receiving a second video data from a second video source at a second video decoder via a second video channel (see Fig. 1);

decoding, via the first video decoder, a first frame of the first video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2);

decoding, via the second video decoder, a second frame of the second video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2);

inputting the first decoded frame (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2, the decoded video signals/frames of Reynolds corresponding to the image inputs of Machida, see Machida, Fig. 3); and

inputting the second decoded frame (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2, the decoded video signals/frames of Reynolds corresponding to the image inputs of Machida, see Machida, Fig. 3).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Machida's system to include the limitations as taught by Reynolds for the same advantage as stated above regarding claim 1.

Machida in view of Reynolds does not specifically disclose transmitting the frame into a first portion of a video buffer for updating the display with the processed first decoded frame;

storing the second frame into a second portion of the video buffer that is not updating the display, or

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Reitmeier discloses transmitting a first frame to a video buffer of a video buffer for updating the display with the processed first decoded frame (see Reitmeier, Fig. 1 and col 3, lines 66-67 and col 4, lines 63-65).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds to include the limitations as disclosed by Reitmeier for the advantage of providing a more efficient system for rapidly acquiring channels.

Machida in view of Reynolds and Reitmeier does not specifically disclose transmitting a first frame into a first portion of a video buffer,

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display, or

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Miyazaki discloses transmitting a first frame into a first portion of a video buffer (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14), and

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Reitmeier to include the limitations as disclosed by Miyazaki for the advantage of reducing the latency of acquiring channels.

Machida in view of Reynolds, Reitmeier and Miyazaki does not specifically disclose providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Mizutome discloses providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines (see Figs. 4 and 20 and related text).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds, Reitmeier and Miyakai to include the limitations as taught by Mizutome for the advantage of providing an improved system capable of combining multiple video signals at a user location to effectively display multiple images in an output mode preferred by a user.

14. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record), Reitmeier (of record), Miyazaki (of record) and Mizutome (previously cited), as applied to claim 14 above, and further in view of Miura (of record).

Regarding claim 15, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome discloses processing, by a first video processing pipeline, a decoded first frame, but does not specifically disclose determining whether a first video source coupled to the first video processing pipeline is in a failed state.

In an analogous art, Miura discloses determining whether a first video source coupled to the first video processing pipeline is in a failed state (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome to include the limitations as disclosed by Miura for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 16, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome, and further in view of Miura discloses processing, by a first video processing pipelines, a first decoded frame comprising outputting a blacked out frame for a first video source upon determining that the first video source is in a failed state (see Miura, col 20, lines 49-54).

Regarding claim 17, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome, and further in view of Miura discloses switching a configuration of a second portion of a video

buffer that is not updating a display with a part of a video buffer that is updating the display, upon determining that the first and second video processing pipelines have completed processing the first and second decoded frames (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 18, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome, and further in view of Miura discloses scaling first and second decoded frames (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7) based on image size and the number of video sources (the number of video sources that are actually to be displayed, see Machida, col 5, lines 32-48).

15. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claim 19 above, and further in view of Miura (of record).

Regarding claim 23, Machida in view of Reynolds and Mizutome discloses a video processing pipeline, but does not specifically disclose executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time.

In an analogous art, Miura discloses executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the

limitations as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 24, Machida in view of Reynolds and Mizutome, and further in view of Miura discloses a video fail operation comprising an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the plurality of video sources (see Miura, col 20, lines 49-54).

Regarding claim 25, Machida in view of Reynolds and Mizutome, and further in view of Miura discloses a video fail operation comprising an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure (see Miura, col 20, lines 49-54 and col 36, lines 20-33).

16. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claim 19 above, and further in view of Kovacevic (of record).

Regarding claim 26, Machida in view of Reynolds and Mizutome does not specifically disclose analog video data.

In an analogous art, Kovacevic discloses analog video data (see [0026], lines 8-11).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as taught by Kovacevic for the advantage of providing an improved system for

displaying multiple images that allows for multiple types of video signals to be received, processed and viewed.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHENEA P. SMITH whose telephone number is (571)272-9524. The examiner can normally be reached on Monday through Friday, 7:30 am - 5:00 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John W. Miller/
Supervisory Patent Examiner, Art Unit 2421

/Chenea P. Smith/
Examiner, Art Unit 2421